Project Proposal

The idea is to create a Jenkins plugin for one of widely used EDA tools. Both ASIC or FPGA design flow are acceptable, the tool should be proposed by the potential student. Open-source EDA tools would be preferable (e.g. Yosys, FuseSoC, ArachnePnR, icetools), but we also consider conditionally-free tools (like FPGA design EDAs).

For example such plugin could report FPGA resource utilization per build as well as the project trend. Other example: timing report trend.

Integrating UVM reports into Jenkins build and project pages is also an example of such plugin.

Skills to study/improve

- Basic knowledge of Jenkins (as a user)
- Basic knowledge of Java programming language

Hands-on experience with the selected EDA tool. In the case of FPGA flows it would be useful to have a prototyping board as well.

Project Metadata

Created on: 2016

Goal: Create a new Jenkins plugin for one of widely used EDA tools.

Champion: Martin d'Anjou

Champion Github Id and link: https://github.com/martinda

Champion Jenkins JIRA/LDAP id: deepchip

Champion Time Zone: UTC-4

Champion Role: I am making this proposal as a mentor

Project Category: plugin SIG/Subproject: HW and EDA

Project Gitter chat room: https://gitter.im/jenkinsci/hw-and-eda-sig

Potential Mentors

The potential mentors are:

- 1) Martin d'Anjou
- 2) Oleg Nenashev
- 3) Mentors could come from the librecores org